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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,366	01/14/2004	Hiroaki Nakano	TAI 146	2358

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,366	NAKANO, HIROAKI	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-36 and 38-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-36,38-41,44 and 46* is/are rejected.

7)☒ Claim(s) *42,43,45 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 44 is rejected under 35 U.S.C. 102(e) as being anticipated by Shibamoto et al. (2002/0105070).

Shibamoto et al. teach in figure 15 and related text a semiconductor device comprising:

a substrate (see paragraph [0036]) having an upper surface including a chip mounting region, a wiring region and a reinforcement layer region, the regions being independent from each other, the wiring region being located outside of the chip mounting region, the reinforcement layer region being located outside of the wiring region;

wiring 10 formed in the wiring region;

a reinforcement layer 3 formed in the reinforcement layer region;

a protective film 8 that covers the substrate, the wiring and the reinforcement layer to protect them;

a semiconductor chip 1 arranged over the chip mounting region and on the protective film;

a bonding wire (part of wiring 10) that connects the semiconductor chip to the wiring; and

a sealing resin (part of film 8 which is adjacent to chip 1) that covers the semiconductor chip and seals at least the bonding wire and the semiconductor chip.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibamoto et al. (2002/0105070) in view of Baba (6,046,077).

Shibamoto et al. teach substantially the entire claimed structure, as applied to claim 44 above, except teaching the connection of the substrate to the device.

Baba teaches in figure 6 and related text solder balls 8 disposed on a lower surface of the substrate 4, wherein said substrate is disposed over the solder balls, and under the wiring, the reinforcement layer, and the semiconductor chip.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the substrate in Shibamoto et al.'s device by using solder balls disposed on a lower surface of the substrate, wherein said substrate is disposed over the solder balls, and under the wiring, the reinforcement layer, and the

semiconductor chip, as taught by Baba, in order to provide good external connections to the device by using conventional solder balls connections.

Claims 31-36 and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba (6,046,077) in view of Jeun et al. (7,061,080).

Baba teaches in figure 6 and related text a semiconductor device comprising:

a substrate 4 having an upper surface including a chip mounting region, a wiring region (the region between the chip 1 and the reinforcement layer 6) and a reinforcement layer region, the regions being independent from each other, the wiring region being located outside of the chip mounting region, the reinforcement layer region being located outside of the wiring region;

a reinforcement layer 6 formed in the reinforcement layer region;

a protective film 3 that is a solder resist, and that is in direct contact with the substrate, and covers the substrate, the wiring region and the reinforcement layer to protect them;

a semiconductor chip 1 arranged over the chip mounting region and on the protective film; and

a sealing resin (part of film 3 located over chip 1) that covers the semiconductor chip and seals at least the bonding wire and the semiconductor chip.

Baba do not teach wiring formed in the wiring region, and a bonding wire that connects the semiconductor chip to the wiring.

Jeun et al. in figure 2 and related text a circuit element 220 formed adjacent to semiconductor chip 221 and a bonding wire 222 that connects the semiconductor chip 221 to the circuit component.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a circuit element adjacent to the semiconductor chip of Baba's device and to use a bonding wire to connect the semiconductor chip to the circuit component, in order to reduce the size of the device by forming a circuit component in the region between the chip and the reinforcement layer.

Note that forming a circuit component in the region between the chip and the reinforcement layer would result in a wiring formed in said region.

Regarding claims 32-36 and 38-39, prior art's device comprises: a protective film has a shape corresponding to the surfaces of the wiring, the reinforcement layer and the substrate,

solder balls provided on a rear surface of the substrate, wherein

the solder balls are electrically connected with the wiring, wherein

the wiring comprises copper, wherein

the solder balls are provided at positions on the rear surface of the substrate corresponding to the wiring region, wherein

the protective film is a solder resist, wherein

a surface of a portion of the protective film positioned in the chip mounting region is planar,

wherein none of the wiring is covered by the semiconductor chip.

Regarding claims 32-36 and 38-39, prior art's device comprises:

a protective film disposed under the semiconductor chip and supports the semiconductor chip over the chip mounting region, with the semiconductor chip being separated from the wiring and from the surface of the substrate by the protective film, the semiconductor chip has a terminal on an upper surface thereof, and wherein said bonding wire that extends from the terminal to the wiring to electrically connect the semiconductor chip to the wiring.

Allowable Subject Matter

Claims 42, 43, 45 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant argues that Shibamoto et al. do not teach a sealing resin that covers the semiconductor chip.

The sealing resin (part of film 8 which is adjacent to chip 1) of Shibamoto et al. covers the side walls and bottom of semiconductor chip. Therefore, Shibamoto et al. teach a sealing resin that covers the semiconductor chip, as claimed.

The rest of applicant's arguments with respect to claims 31-36 and 38-47 have been considered but are moot in view of the new ground(s) of rejection, and the objection to claims 42, 43, 45 and 47.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
12/23/06

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PRIMARY EXAMINER
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